EE/CPRE/SE 4920 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 4

10/4/2024 - 10/31/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

After much trial and suffering precheck has finally been worked out and a tutorial has been created to help alleviate the pain for future students that work on this project. There was also progress made into creating the C code necessary for the ReRAM operations to be run by the processor.

Past Week Accomplishments:

- Modeled the full ReRAM array
- Library for array functions completed – testing still needed
- SNR calculations done
- Determined method of script assisted layout for ADC comparator
- ADC Schematic is done
- Nmos parameters extracted from NGspice

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Modeled ReRAM array created more documentation to assist future teams	15	141
Gage Moorman	Created lookup table for MOS devices to help optimize TIA and ADC. Completed ADC schematic. Recharacterized parameters to be compatible with a lookup table for the sky130 process. Sketched what the layout out for the Comparator should be	15	100
Nathan Cook	Function library finished SNR calculations done	14	94
Jason Xie	Finished implementing Priority Encoder and assisted in finishing complete ADC simulations. Assisted in creating a GMID lookup table for TIA sizing. Explored options for tcl	20	103

	based Magic layout methods.		

Pending Issues:

- Test ReRAM functions
- Double check SNR calculations
- Script assisted transistor placement is feasible with TCL and Python, but auto-routing is still an issue
- Having issue with Xschemrc and ngspice identifying the correct subcircuit netlist

Plans for the coming week:

- Gage Moorman
  - Build upon analog documentation
  - Do ADC matching analysis
  - Finish lookup table and design TIA
  - Do Monte Carlo analysis for ADC design
  - Do full integration testing with ADC and TIA
- Konnor Kivimagi
  - Continue implementing multiple components to pass precheck together.
  - Help out where needed.
- Nathan Cook
  - Write test cases for ReRAM functions
  - Redo SNR values
  - Help others when done
- Jason Xie
  - Work on comparator layout
  - Explore analogue and digital blackbox module hardening

Summary of Advisor Meeting:

Discussed our current progress and what we plan to complete in the coming weeks. We also discussed deliverables and what may be achievable and not achievable.